ALLOWANCE

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with John A. Lingl (Reg. #57,414) on 5/13/2010.

The application has been amended as follows:

In the Specification

3. In the specification filed 2/28/2005, please amend the Title:

In the Title:

replace: "Process and device for the verification of digital circuits", with - - Method and device for verifying digital circuits - -.

(This Examiner's amendment has been made in order to place the application in a condition for allowance)

Reasons For Allowance

4. The following is an examiner's statement of reasons for allowance:

Claims 1, 5-7 and 9-17 are allowed because the prior art made of record does not teach or suggest a method/apparatus/computer-program-product for verifying digital circuits, in the manner as recited in the claims.

5. With respect to claims 1, 5-7 and 9-17, the prior art fails to teach the combination of steps in claims 1, and similar claims 14, 16 and 17, including the following particular steps as recited in claims 1, 14, 16 and 17:

providing an alternative reference description for the use in verification of digital circuits by using a computer, wherein in the verification a digital circuit to be verified is compared with a reference description of the digital circuit, in order to recognize errors in the digital circuit using an equivalence test, wherein for at least one specific circuit structure described by a reference description of the digital circuit a plurality of different pre- defined implementation alternatives is known, the method comprising the computer implemented steps of:

(a) determining, for each one of the at least one specific circuit structure first implementation alternative out of the plurality of the different pre- defined implementation alternatives, such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified compared to other implementation alternatives out of the plurality of the different pre-defined implementation alternatives and whereby each one of the plurality of the different pre-defined implementation alternatives is simulated respectively, using random pattern simulation, and compared with a corresponding simulation of the digital circuit, in order to determine the first implementation alternative having the highest degree of structural

equivalence with the digital circuit, the implementation alternative out of the plurality of the different pre-defined implementation alternatives, which, under the random pattern simulation, has the largest number of equivalent design points with the digital circuit,

(b) replacing in the reference description of the digital circuit, the description of the individual circuit structures by the first implementation alternative determined for the respective circuit structure in step (a) having the highest degree of structural equivalence in each case to obtain the alternative reference description, and

(c) outputting the alternative reference description for use as a reference description in the verification of the digital circuit,

wherein the at least one specific circuit structure, for which in step (a) the first implementation alternative with the highest degree of structural equivalence is determined in each case, are multiplier structures for realizing integral multiplication functions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUCHIN PARIHAR whose telephone number is (571)272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suchin Parihar/
Examiner, Art Unit 2825

/Jack Chiang/

Supervisory Patent Examiner, Art Unit 2825